

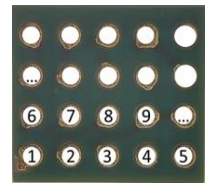
System-in-Package (SiP)

J10 Introduction

J10 System-In-Package (J10 SIP) is a complete solution with 20Pin that provides the easiest way to Integrate the industry's lowest power Bluetooth low energy technology into a wireless application. The chip solution can support diversity applications, challenged by package size, power consumption and wireless feature, for the applications, such as coin cell battery powered, long cycle life, portable with mobility, J10 chip is one of the best candidate solutions, to support customized system requesting Bluetooth-Low-Energy, miniaturization, and ultra-lowest power consumption features.



Top View



Bottom View

Order information

Device	Package	Shipping
J10HAOTC	4mm*3.5mm (20pin)	3000 / Tape & Reel
Note: please refer to sales@jhearing.com for more information		

The J10 SIP contains a radio SoC and all necessary passive components in one package, to help miniaturized System-in-Package (SiP) solutions for the medical microelectronics industry.

Important Notice and Warnings

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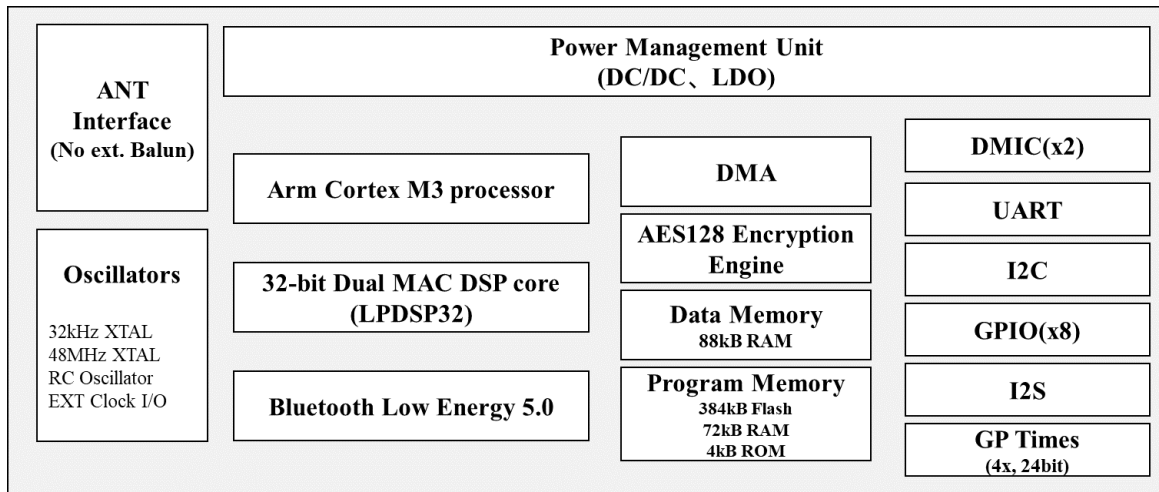
1.1 Key Benefits

- Industry ultra-lowest power consumption support long battery life applications
- Bluetooth low energy technology certified 5.0 for wireless feature
- Smallest BLE wireless module size support limited system size applications
- M3 and DSP dual-core system architecture
- Broadcast audio streaming features with competitive low latency audio
- Custom audio protocol to support low power audio streaming from a remote dongle
- Function blocks integrated turnkey solution
- Embedded Flash
- Integrates medical application features for fast time-to-market

Notice:

All specifications for the J10 System-in-Package are based on the RSL10 radio SoC. The J10 SIP data sheet only contains key parameters. For a full list of RSL10 parameters and specifications, refer to the RSL10 data sheet

2.Sub-system overview



2.1 Arm Cortex–M3 Processor

The Arm Cortex–M3 processor subsystem includes the Arm Cortex–M3 processor, which is the master processor of the J10 chip. It also contains the Bluetooth baseband controller, and all interfaces and other peripherals.

The Arm Cortex–M3 processor is a state-of-the-art 32-bit core with embedded multiplier and ALU for handling typical control functions. Software development is done in C. It features a low gate count, low interrupt latency, and low-cost debug functionality. It is primarily intended for deeply embedded applications that require low power consumption with fast interrupt response. The processor implements the Arm architecture v7–M. For power management, the processor can be placed under firmware control, into a Standby mode, in which the processor clock is disabled. The Nested Vectored Interrupt Controller (NVIC) will continue to run to enable exiting Standby mode on an interrupt.

2.2 LPDSP32

LPDSP32 is a C-programmable, 32-bit DSP developed by ON Semiconductor. LPDSP32 is a high efficiency, dual Harvard DSP that supports both single (32-bit) and double precision (64-bit) arithmetic. LPDSP32's dual MAC unit, load store architecture is specifically optimized to support audio processing tasks. The advanced architecture also provides:

- Two 72-bit ALUs capable of doing single and double precision arithmetic and logical operations

- Two 32-bit integer/fractional multipliers
- Four 64-bit accumulators with 8-bit overflow (extension bits) LPDSP32 can typically support the audio codecs needed to deploy audio device communication use cases. This includes (but is not limited to) codecs to support:
- A 16 kHz sample rate, producing a signal with a 7 kHz bandwidth (E.g.; G.722 and mSBC codec)
- A 24 kHz sample rate, producing a signal with an 11 kHz bandwidth (E.g.: G.722, CELT codec from the OPUS standard)

Communications to the Arm Cortex-M3 processor are completed via interrupts and shared memories. Software development is done in C, and the development tools are provided upon request from Synopsys.

2.3 Interfaces

- Two independent SPI interfaces that can be configured in master and slave mode
- A fully configurable PCM interface
- A standard general purpose I2C interface
- A standard general purpose UART interface
- Two PWM (Pulse Width Modulation) drivers that can
- generate a single bit output signal at a given frequency
- A two-channel digital microphone (DMIC) input
- An output driver (OD) to allow direct connection to high impedance speakers
- SWJ-DP interface for the Arm Cortex-M3 processor
- JTAG interface for the Arm Cortex-M3 processor,
- internal Flash memory, and the LPDSP32
- J10 includes 8 DIO pads (Digital Input/Output) that all can be assigned to any of the interfaces above or used as general purpose DIOs.

2.4 Peripherals

- Four general purpose timers
- A DMA (Direct Memory Access) controller to transfer data between peripherals and memories without any core intervention

- A flash copier to initialize SRAM memories and that can be used with the CRC blocks to validate flash memory contents
- An Analog to Digital converter (ADC), accessed by the Arm Cortex–M3 processor. The ADC can read 4 external values (DIO[0]–DIO[3]), AOUT, VDDC, VBAT/2 and the ADC offset value.
- Two standard Cyclic Redundancy Code (CRC) blocks to ensure data integrity of the user application code and data
- An Asynchronous Sample Rate Converter (ASRC) and Audio Sink Clock Counters blocks to provide a means of synchronizing the audio sample rate between the radio link and the host device
- A Watchdog timer to detect and recover from RSL10 malfunctions.
- Four autonomous 32–bit Activity Counters. These counters help analyze how long the system has been running and how much the Arm Cortex–M3 processor, LPDSP32, and the flash memory have been used by the application. This is useful information to estimate and optimize the power consumption of the application. An IP protection system to ensure that the flash content cannot be copied by a third party. It can be used to prevent any core or memory of the RSL10 from being accessed externally after the RSL10 has booted.
- Program memory loop caches for each processor to reduce the RSL10 power consumption. This reduces the number of flash and RAM memory accesses by caching the program words that are read in these loops.

3.Applications

J10 chip can be used for diversity applications, which need smallest package size, ultra-low power consumption and wireless featured.

- Blood gas analyzers
- ECG patient monitoring systems
- Continued blood glucose monitoring
- Vital sign monitoring
- Heart rate monitors
- Pulse oximetry
- Automated External Defibrillator (AED)
- Diabetes Management device: BGM, CGM, Insulin pump

3.1 Portable Medical device applications

The J10 system can support most of portable medical device applications, such as heart rate monitoring, diabetes management BGM, CGM device, hearing loss assistance device etc.

The reference design shown in Figure 3.1 is for one of the portable medical device applications, which as turkey solution for OTC hearing aid application system architecture, no additional external components request but the speaker and Michonne, the key notes as below:

- J10 chip interested keys components for hearing aid applications, few external components requirement
- The programing interface support customize hearing aid algorithms from diversity requirements
- BLE wireless feature embedded support smartphone interface, support mobile phone App remote fitting feature
- Reserve antenna port for customer flexible antenna design necessary
- Customized audio streaming protocol support low-latency audio

Typical Application:

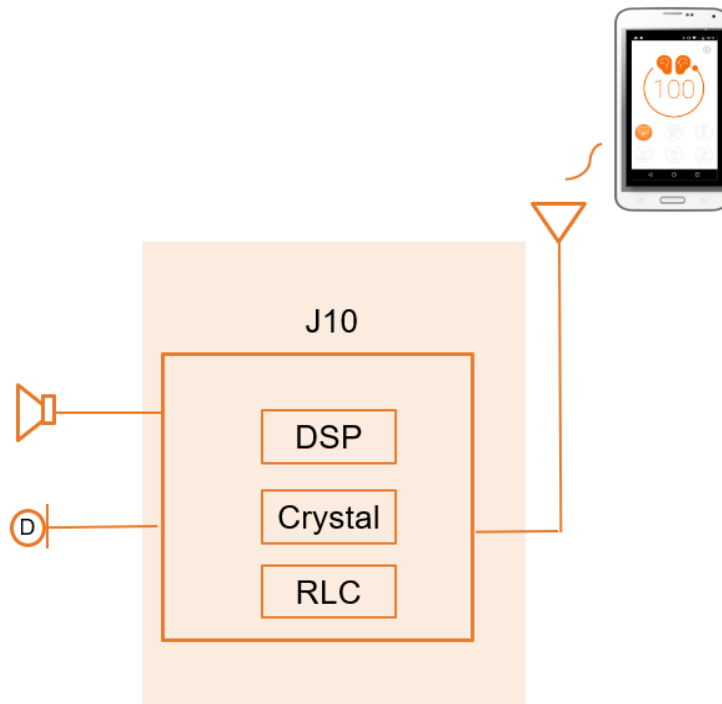


Figure 1 A typical hearing device with J10 (monaural) diagram (Audio streaming supported)

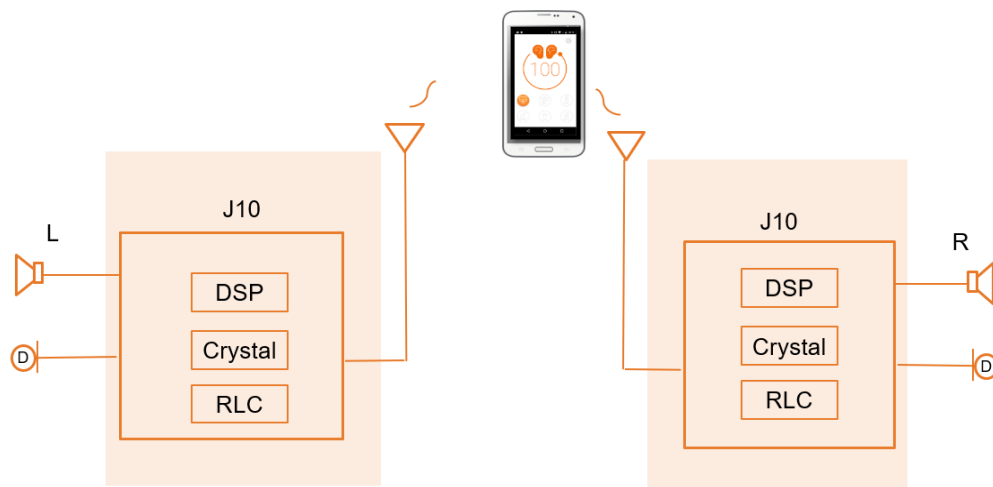


Figure 2 A typical hearing device with J10 (Binaural) diagram (Binaural Audio streaming supported)

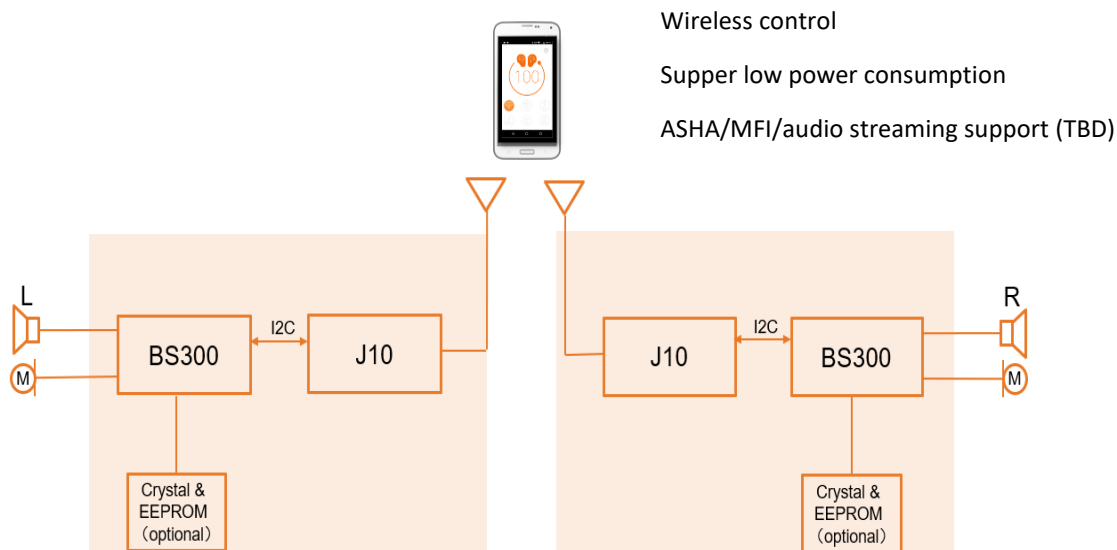
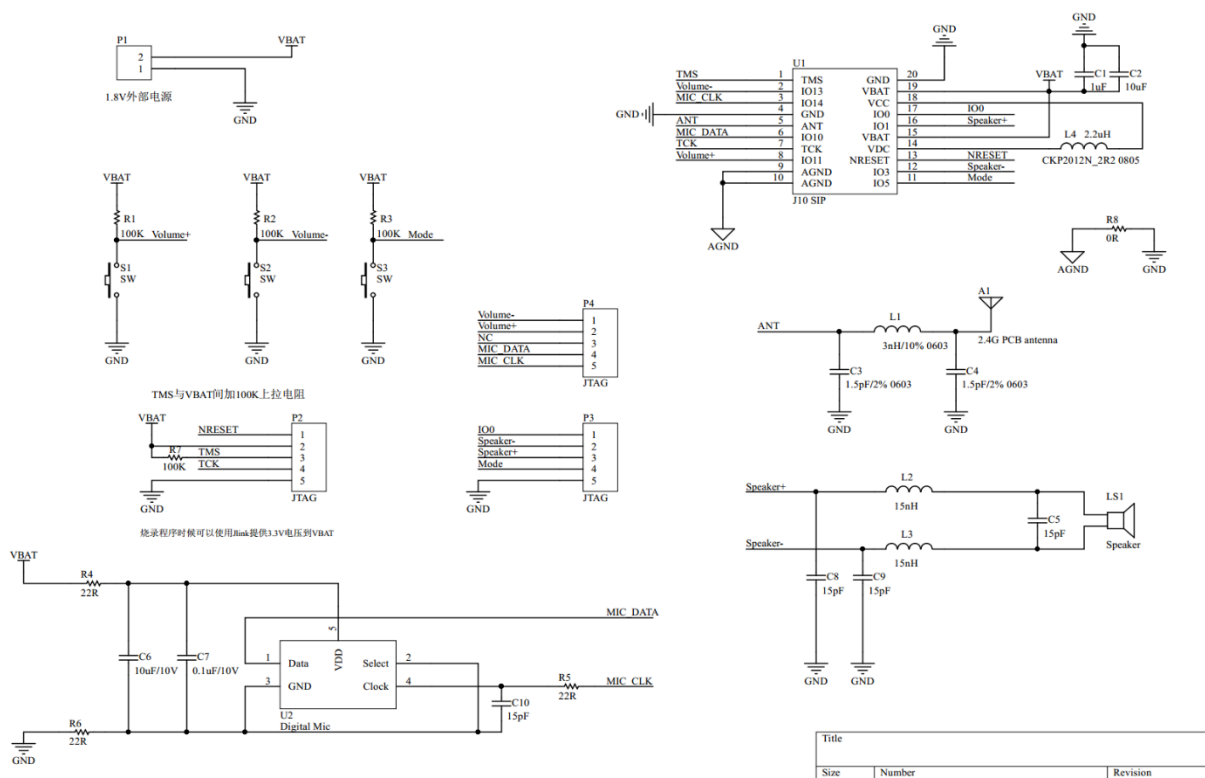


Figure 3 A typical hearing device with B300+J10



3.2 Portable Fitness and wellness Applications

- Sports and activity monitors
- Heart rate monitors
- Smart clothing
- Sleep sensors
- BMI and life vitals

3.3 Infotainment

- Smart watches
- Augmented reality headsets
- Smart glasses
- Wearable imaging devices

4.General Description

4.1 Block Diagram

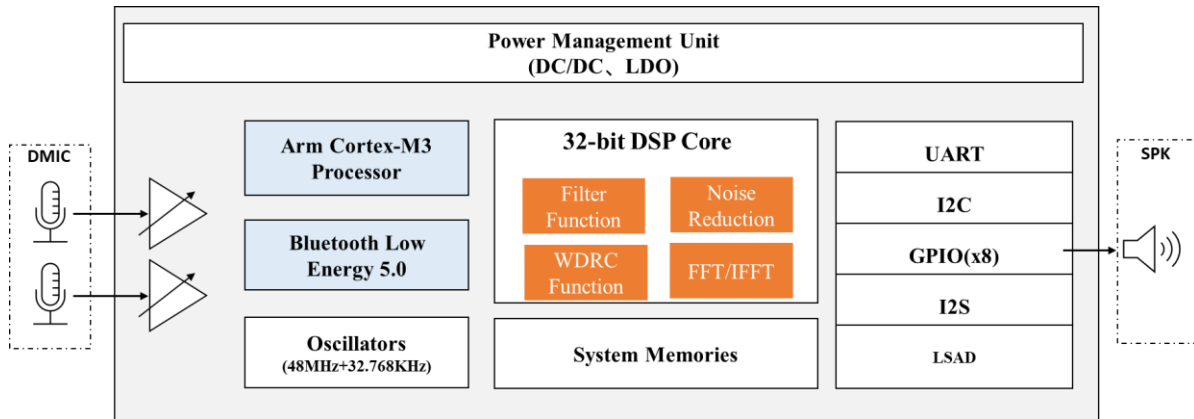


Figure 4.1 J10 Diagram Blocks

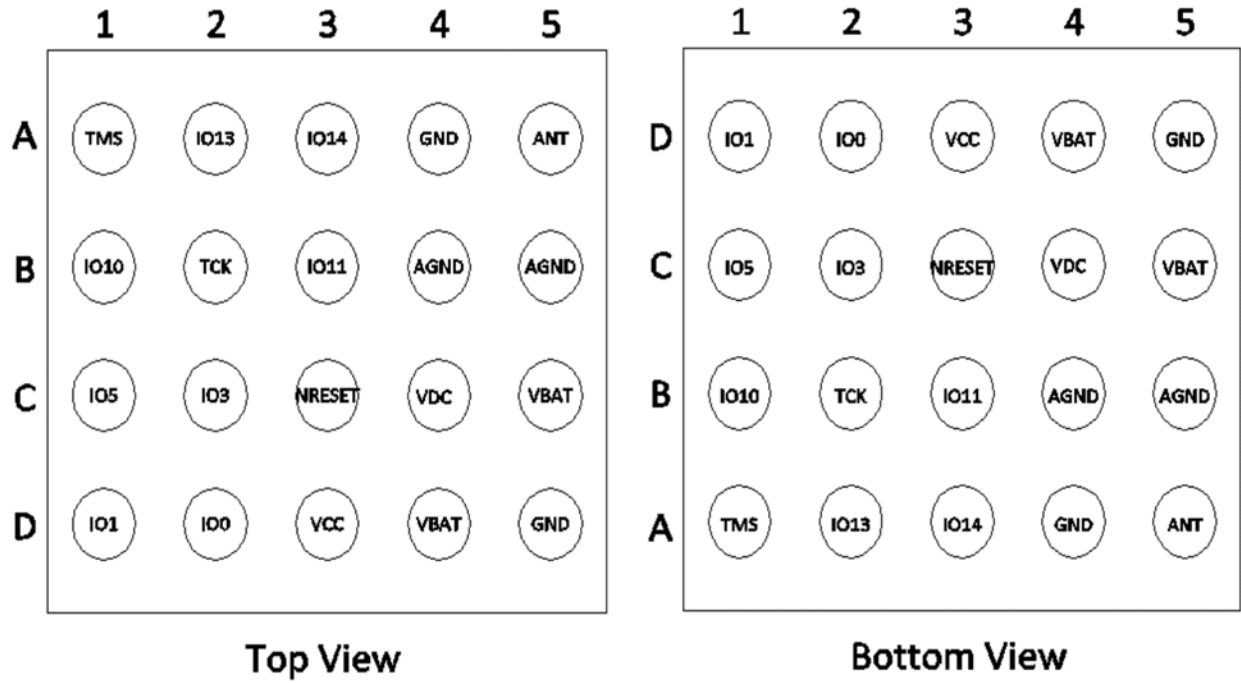
5. Electrical Characteristics

Refer the RSL10 spec for detail.

(<https://www.onsemi.com/download/data-sheet/pdf/rsl10-d.pdf>)

6. Pin layout view and Pin Description

6.1 Pin layout view



6.2 Pin Description

Pin#	Pin Def	Pin Name	Pin Function	Pin Description
1	A1	TMS	I/O	Test Mode Select
2	A2	IO13	I/O	I/O
3	A3	IO14	I/O	I/O
4	A4	GND	GND	GND
5	A5	ANT	RF	RF signal input/output (Antenna)
6	B1	IO10	I/O	I/O
7	B2	TCK	I/O	External clock input
8	B3	IO11	I/O	I/O
9	B4	AGND	AGND	AGND
10	B5	AGND	AGND	AGND
11	C1	IO5	I/O	I/O
12	C2	IO3	I/O	I/O
13	C3	NRESET	I/O	Reset
14	C4	VDC	VDC	DC–DC output voltage to external LC filter
15	C5	VBAT	Power Source	Power Source
16	D1	IO1	I/O	I/O
17	D2	IO0	I/O	I/O
18	D3	VCC	VCC	DC–DC filtered output
19	D4	VBAT	VBAT	VBAT
20	D5	GND	GND	GND

7.PCB Guidelines and SMT Guidelines

7.1 PCB Design Guidelines

1. Decoupling capacitors should be placed as close to the related balls as possible.
2. Differential output signals should be routed as symmetrically as possible.
3. Analog input signals should be shielded as well as possible.
4. Pay close attention to the parasitic coupling capacitors.
5. Special care should be made for PCB design in order to obtain good RF performance.
6. Multi-layer PCB should be used with a keep-out area on the inner layers directly below the antenna matching circuit in order to reduce the stray capacitances that influence RF performance.
7. All the supply voltages should be decoupled as close as possible to their respective pin with high performance RF capacitors. These supplies should be routed separately from each other and if possible on different layers with short lines on the PCB from the chip's pin to the supply source.
8. Digital signals shouldn't be routed close to the crystal or the power supply lines.
9. Proper DC-DC component placement and layout is critical to RX sensitivity performance in DC-DC mode.

7.2 SMT Solder Information

The RSL10 SIP is constructed with all RoHS compliant material and should be reflowed accordingly. This device is Moisture

Sensitive Class MSL3 and must be stored and handled accordingly. Re-flow according to IPC/JEDEC standard J-STD-020C,

Joint Industry Standard: Re-flow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. Hand soldering is not recommended for this part.

For more information, see SOLDERRM/D available from www.onsemi.com.

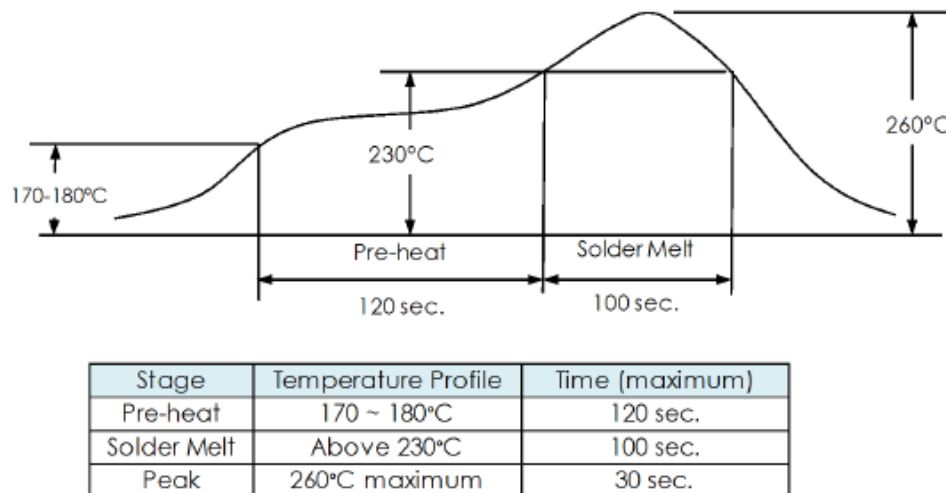
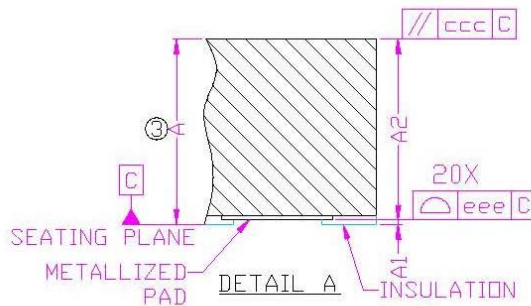
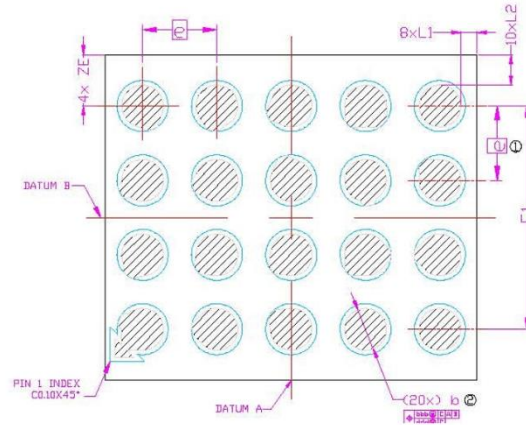
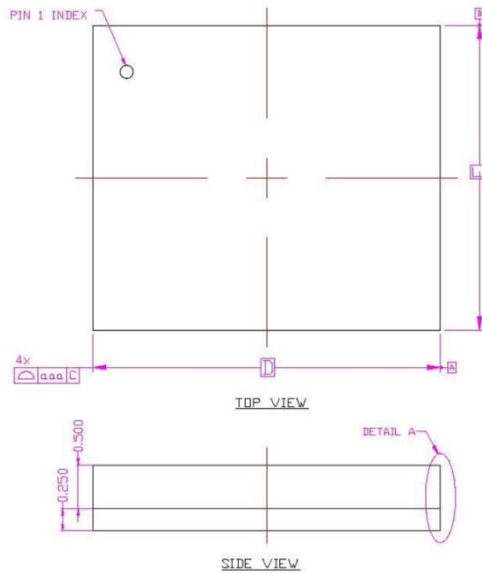


Figure 7.1 SOLDER FLOW PROFILE

8.Package Outline

REV	DESCRIPTION	DATE	DESIGNER	REVIEWER	APPROVER
A	Initial Release	2022-MAR-04	Nancy.Jiang	DENNIS	JI HAIJIAN



DIMENSIONAL REFERENCES				unit: mm
REF.	Min.	Nom.	Max.	
A	0.69	0.75	0.81	
A1	-	-	0.03	
A2	-	-	0.78	
b	0.40	0.45	0.50	
D	3.95	4.00	4.05	
E	3.45	3.50	3.55	
E1	2.40 BSC			
ZE	0.55 BSC			
e	0.80 BSC			
L1	0.125	0.175	0.225	
L2	0.275	0.325	0.375	

DIMENSIONAL REFERENCES		unit: mm
REF.	TOLERANCE OF FORM AND POSITION	
aaa	0.10	
bbb	0.10	
ccc	0.10	
ddd	0.08	
eee	0.08	

Notes :

- 'e' REPRESENTS THE BASIC TERMINAL PITCH.
SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.
- DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.
- DIMENSION 'A' INCLUDES PACKAGE WARPAGE.
- EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.
- PACKAGE DIMENSIONS TAKE REFERENCE TO JEDEC MO-208 REV.C.

9.Ordering Information

Contact: sales@jhearing.com

PUBLICATION ORDERING INFORMATION

TECHNICAL SUPPORT tech@jhearing.com **Email Requests to** sales@jhearing.com **Website** www.jhearing.com