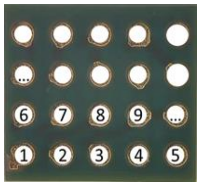
System-in-Package (SiP)

J10 Introduction

J10 System−In−Package (J10 SIP) is a complete solution with 20Pin that provides the easiest way to Integrate the industry's lowest power Bluetooth low energy technology into a wireless application. The chip solution can support diversity applications, challenged by package size, power consumption and wireless feature, for the applications, such as coin cell battery powered, long cycle life, portable with mobility, J10 chip is one of the best candidate solutions, to support customized system requesting Bluetooth-Low-Energy, miniaturization, and ultra-lowest power consumption features.

Top View



Bottom View

Order information

Device	Package	Shipping
J10HAOTC	4mm*3.5mm (20pin)	3000 / Tape & Reel
Note: please refer to sales@jhearing.com for more information		

The J10 SIP contains a radio SoC and all necessary passive components in one package, to help miniaturized System-in-Package (SiP) solutions for the medical microelectronics industry.

Important Notice and Warnings

The information given in this document shall not be regarded as a guarantee of conditions or characteristics. With respect to any typical values stated and any information regarding the application of the product, Jhearing hereby disclaims all warranties and liabilities of any kind, including without limitation warranties of non-infringement of intellectual property rights of any third party. The data contained in this document is exclusively intended for skilled developers to evaluate the suitability of the product for the intended application, and other reproduction and display of these information or related resources is prohibited.

Except as otherwise approved by Jhearing, Jhearing' products may not be used in any applications where a failure of the product or any consequences of the use can reasonably be expected to result in personal injury.

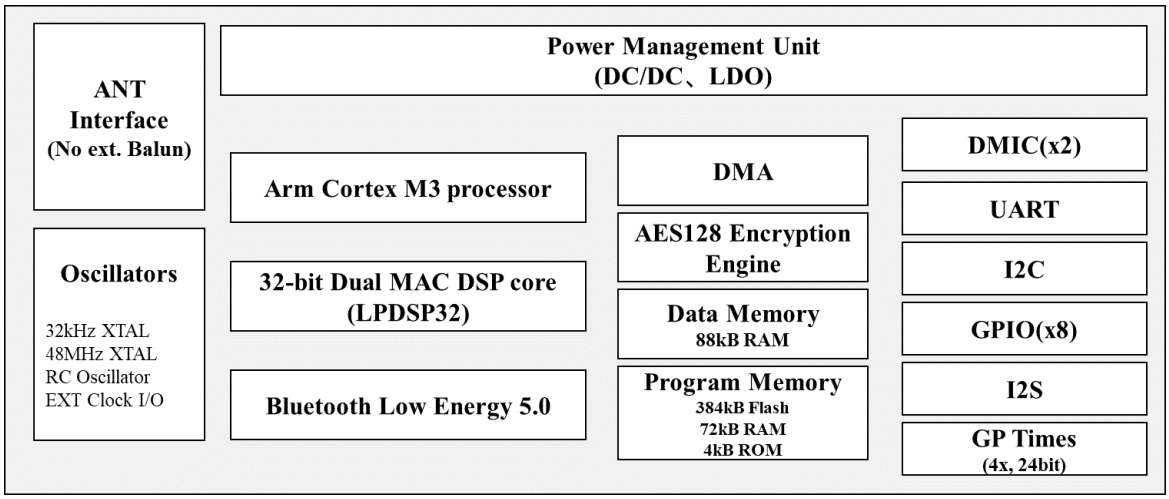
1.1 Key Benefits

- Industry ultra-lowest power consumption support long battery life applications
- Bluetooth low energy technology certified 5.0 for wireless feature
- Smallest BLE wireless module size support limited system size applications
- M3 and DSP dual-core system architecture
- Broadcast audio streaming features with competitive low latency audio
- Custom audio protocol to support low power audio streaming from a remote dongle
- Function blocks integrated turnkey solution
- Embedded Flash
- Integrates medical application features for fast time-to-market

Notice:

All specifications for the J10 System−in−Package are based on the RSL10 radio SoC. The J10 SIP data sheet only contains key parameters. For a full list of RSL10 parameters and specifications, refer to the RSL10 data sheet

2.Sub-system overview



2.1 Arm Cortex−M3 Processor

The Arm Cortex−M3 processor subsystem includes the Arm Cortex−M3 processor, which is the master processor of the J10 chip. It also contains the Bluetooth baseband controller, and all interfaces and other peripherals.

The Arm Cortex−M3 processor is a state−of−the−art 32−bit core with embedded multiplier and ALU for handling typical control functions. Software development is done in C. It features a low gate count, low interrupt latency, and low−cost debug functionality. It is primarily intended for deeply embedded applications that require low power consumption with fast interrupt response. The processor implements the Arm architecture v7−M. For power management, the processor can be placed under firmware control, into a Standby mode, in which the processor clock is disabled. The Nested Vectored Interrupt Controller (NVIC) will continue to run to enable exiting Standby mode on an interrupt.

2.2 LPDSP32

LPDSP32 is a C−programmable, 32−bit DSP developed by ON Semiconductor. LPDSP32 is a high efficiency, dual Harvard DSP that supports both single (32−bit) and double precision (64−bit) arithmetic. LPDSP32's dual MAC unit, load store architecture is specifically optimized to support audio processing tasks. The advanced architecture also provides:

- Two 72−bit ALUs capable of doing single and double precision arithmetic and logical operations

- Two 32−bit integer/fractional multipliers
- Four 64−bit accumulators with 8−bit overflow (extension bits) LPDSP32 can typically support the audio codecs needed to deploy audio device communication use cases. This includes (but is not limited to) codecs to support:
- A 16 kHz sample rate, producing a signal with a 7 kHz bandwidth (E.g.; G.722 and mSBC codec)
- A 24 kHz sample rate, producing a signal with an 11 kHz bandwidth (E.g.: G.722, CELT codec from the OPUS standard)

Communications to the Arm Cortex−M3 processor are completed via interrupts and shared memories. Software development is done in C, and the development tools are provided upon request from Synopsys.

2.3 Interfaces

- Two independent SPI interfaces that can be configured in master and slave mode
- A fully configurable PCM interface
- A standard general purpose I2C interface
- A standard general purpose UART interface
- Two PWM (Pulse Width Modulation) drivers that can
- generate a single bit output signal at a given frequency
- A two−channel digital microphone (DMIC) input
- An output driver (OD) to allow direct connection to high impedance speakers
- SWJ−DP interface for the Arm Cortex−M3 processor
- JTAG interface for the Arm Cortex−M3 processor,
- internal Flash memory, and the LPDSP32
- J10 includes 8 DIO pads (Digital Input/Output) that all can be assigned to any of the interfaces above or used as general purpose DIOs.

2.4 Peripherals

- Four general purpose timers
- A DMA (Direct Memory Access) controller to transfer data between peripherals and memories without any core intervention

- A flash copier to initialize SRAM memories and that can be used with the CRC blocks to validate flash memory contents
- An Analog to Digital converter (ADC), accessed by the Arm Cortex−M3 processor. The ADC can read 4 external values (DIO[0]−DIO[3]), AOUT, VDDC, VBAT/2 and the ADC offset value.
- Two standard Cyclic Redundancy Code (CRC) blocks to ensure data integrity of the user application code and data
- An Asynchronous Sample Rate Converter (ASRC) and Audio Sink Clock Counters blocks to provide a means of synchronizing the audio sample rate between the radio link and the host device
- A Watchdog timer to detect and recover from RSL10 malfunctions.
- Four autonomous 32−bit Activity Counters. These counters help analyze how long the system has been running and how much the Arm Cortex−M3 processor, LPDSP32, and the flash memory have been used by the application. This is useful information to estimate and optimize the power consumption of the application. An IP protection system to ensure that the flash content cannot be copied by a third party. It can be used to prevent any core or memory of the RSL10 from being accessed externally after the RSL10 has booted.
- Program memory loop caches for each processor to reduce the RSL10 power consumption. This reduces the number of flash and RAM memory accesses by caching the program words that are read in these loops.

2.5 Memory Structure

Table 2.1 lists the memory structures attached to J10, and the size and width of each memory structure.

Table 2.1. J10 MEMORY STRUCTURES

Memory Type	Data Width	Memory Size	Accessed by
Program memory (ROM)	32	4 kB	Arm Cortex−M3 processor
Program memory (RAM)	32	4 instances of 8 kB	Arm Cortex−M3 processor
Program memory (RAM)	40	4 instances of 10 kB	LPDSP32 / Arm Cortex−M3 processor
Data memory (RAM)	32	1 instances of 8 kB	Arm Cortex−M3 processor
Data memory (RAM)	32	2 instances of 8 kB	Arm Cortex−M3 processor / LPDSP32
Data memory (RAM)	32	6 instances of 8 kB	LPDSP32 / Arm Cortex−M3 processor
Data memory (RAM)	32	2 instances of 8 kB	Baseband / Arm Cortex−M3 processor
Flash	32	384 kB	Arm Cortex−M3 processor / Flash copier

3.Applications

J10 chip can be used for diversity applications, which need smallest package size, ultra-low power consumption and wireless featured.

- Blood gas analyzers
- ECG patient monitoring systems
- Continued blood glucose monitoring
- Vital sign monitoring
- Heart rate monitors
- Pulse oximetry
- Automated External Defibrillator (AED)
- Diabetes Management device: BGM, CGM, Insulin pump

3.1 Portable Medical device applications

The J10 system can support most of portable medical device applications, such as heart rate monitoring, diabetes management BGM, CGM device, hearing loss assistance device etc.

The reference design shown in Figure 3.1 is for one of the portable medical device applications, which as turkey solution for OTC hearing aid application system architecture, no additional external components request but the speaker and Michonne, the key notes as below:

- J10 chip interested keys components for hearing aid applications, few external components requirement
- The programing interface support customize hearing aid algorithms from diversity requirements
- BLE wireless feature embedded support smartphone interface, support mobile phone App remote fitting feature
- Reserve antenna port for customer flexible antenna design necessary
- Customized audio streaming protocol support low-latency audio

Typical Application:

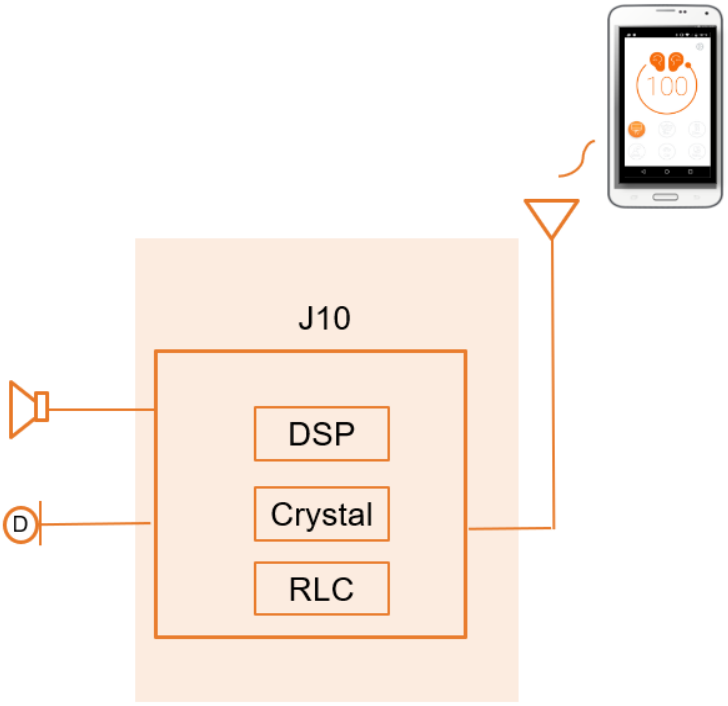


Figure 1 A typical hearing device with J10 (monaural) diagram (Audio streaming supported)

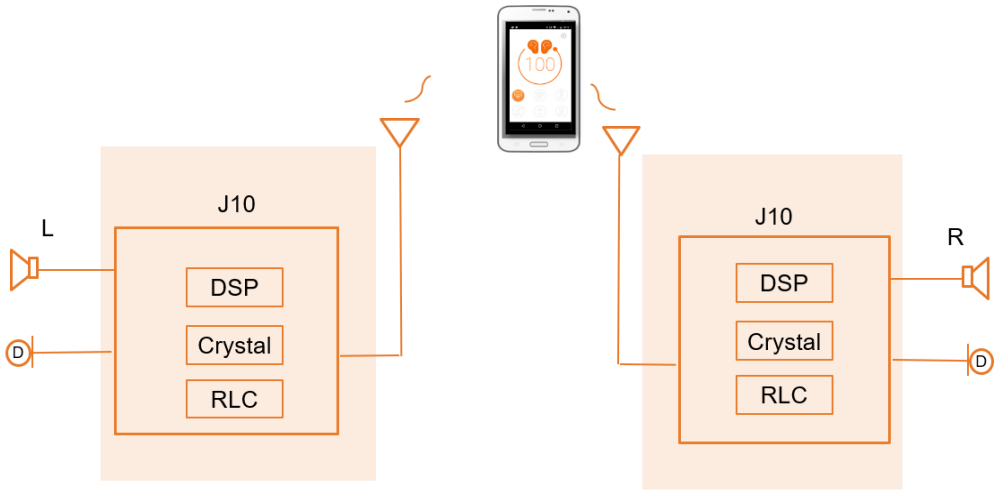


Figure 2 A typical hearing device with J10 (Binaural) diagram(Binaural Audio streaming supported)

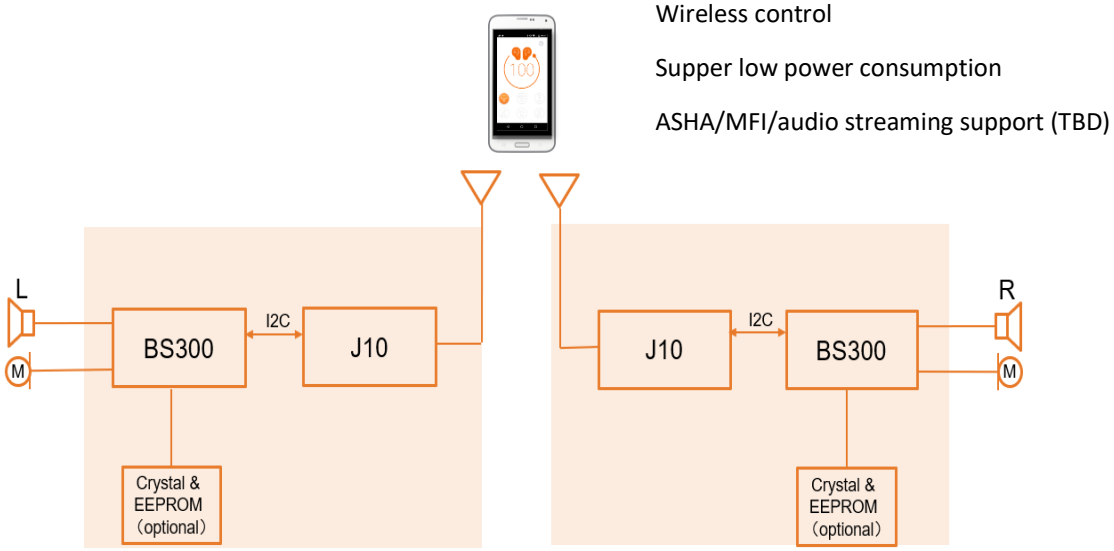


Figure 3 A typical hearing device with B300+J10

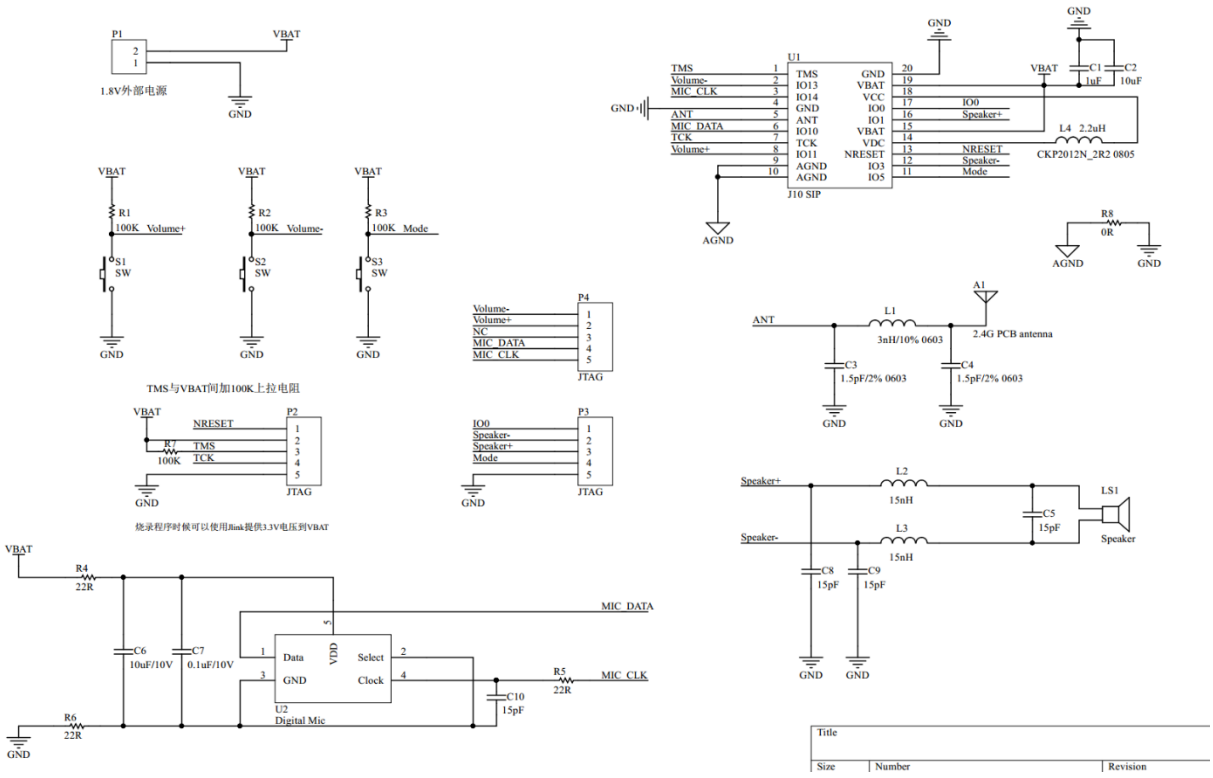


Figure 3.1 Referenced design of hearing-aid (EVB)

3.2 Portable Fitness and wellness Applications

- Sports and activity monitors
- Heart rate monitors
- Smart clothing
- Sleep sensors
- BMI and life vitals

3.3 Infotainment

- Smart watches
- Augmented reality headsets
- Smart glasses
- Wearable imaging devices

4.General Description

4.1 Block Diagram

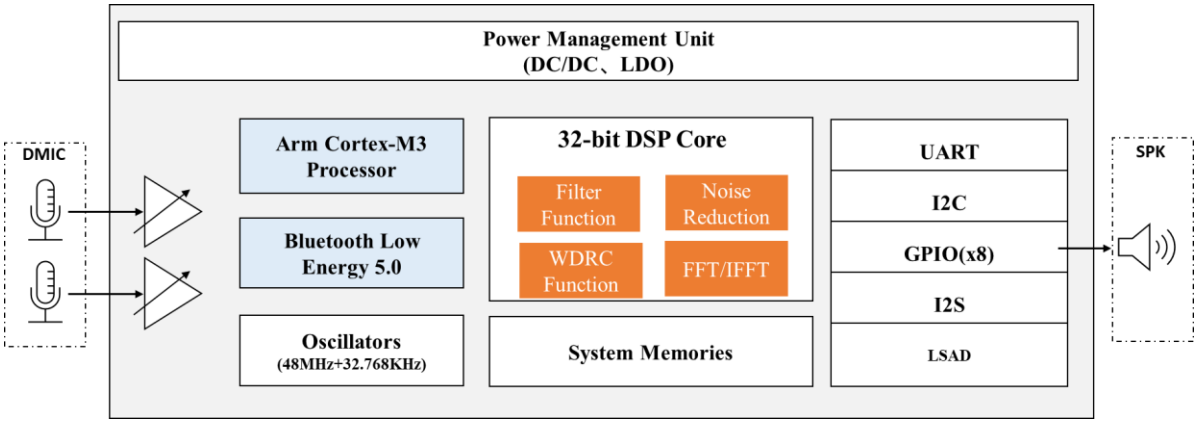


Figure 4.1 J10 Diagram Blocks

4.2 Description（TBD）

5.Electrical Characteristics

5.1 Absolute Maximum Ratings

Table 5.1. ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Min	Max	Unit
VBAT	Power supply voltage		1. 3.63	V
VDDO	I/O supply voltage (Notes 1 and 2)		3.63	V
VSSRF	RF front−end ground	−0.3		V
VSSA	Analog ground	−0.3		V
VSSD	Digital core and I/O ground	−0.3		V
Vin	Voltage at any input pin	VSSD−0.3	VDDO+0.3 (Up to a maximum of 3.63 V)	V
T functional	Functional temperature range	−40	85	□C
T storage	Storage temperature range	−40	85	□C
Caution: Class 2 ESD Sensitivity, JESD22−A114−B (2000 V) The QFN package meets 450 V CDM level				

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

VDDO voltage must not be applied before VBAT voltage on cold start.

For applications where VBAT and VDDO are connected externally (typical connection approach) there is an initial, small power surge during VBAT rise, i.e. cold start of RSL10. This power surge corresponds to:

900 µC max @ VBAT = 3 V

240 µC max @ VBAT = 1.5 V

− 180 µC max @ VBAT = 1.25 V

The power surge can be prevented if there is a minimum delay of 5 ms between the supply voltage reaching 1 V on the VBAT pin, and the supply voltage reaching 1 V on the VDDO pin. This assumes a 4.7 µF capacitor on VCC.

Table 5.2 RECOMMENDED OPERATING CONDITIONS

Description	Symbol	Conditions	Min	Typ	Max	Units
Supply voltage operating range	VBAT	Input supply voltage on VBAT pin (Note 3)	1.18	1.25	3.3	V

Functional operation above the stresses listed in the Recommended Operating Ranges is not implied. Extended exposure to stresses beyond the Recommended Operating Ranges limits may affect device reliability.

In order to be able to use a VBAT Min of 1.1 V, the following reduced operating conditions should be observed:

Maximum Tx power 0 dBm.

SYSCLK □ 24 MHz.

Functional temperature range limited to 0−50 deg C The following trimming parameters should be used:

− VCC = 1.10 V

VDDC = 0.92 V

VDDM = 1.05 V, will be limited by VCC at end of battery life

VDDRF = 1.05 V, will be limited by VCC at end of battery life. VDDPA should be disabled

RSL10 should enter in end−of−battery−life operating mode if VCC falls below 1.03 V. VCC will remain above 1.03 V if VBAT □ 1.10 V under the restricted operating conditions described above.

Table 5.3 ELECTRICAL PERFORMANCE SPECIFICATIONS

Unless otherwise noted, the specifications mentioned in the table below are valid at 25□C for VBAT = VDDO = 1.25 V in LDO mode, or VBAT = VDDO = 3 V in DC−DC (buck) mode.

Description	Symbol	Conditions	Min	Typ	Max	Units
Current consumption RX, VBAT = 1.25 V, low latency	I_{VBAT}			1.8		mA
Current consumption TX, VBAT = 1.25 V, low latency	I_{VBAT}			1.8		mA
Current consumption RX, VBAT = 1.25 V	I_{VBAT}			1.15		mA
Deep sleep current, example 1, VBAT = 1.25 V	Ids1	Wake up from wake up pin or DIO wake up.		50		nA
Deep sleep current, example 2, VBAT = 1.25 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.		90		nA
Deep sleep current, example 3, VBAT = 1.25 V	Ids3	As Ids2 but with 8 kB RAM data retention.		300		nA
Standby Mode current, VBAT = 1.25 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.		30		µA
Current consumption RX, VBAT = 3 V	I_{VBAT}			0.9		mA

Current consumption TX, V_{BAT} = 3 V	I_{VBAT}			0.9		mA
Deep sleep current, example 1, V_{BAT} = 3 V	Ids1	Wake up from wake up pin or DIO wake up.		25		nA
Deep sleep current, example 2, V_{BAT} = 3 V	Ids2	Embedded 32 kHz oscillator running with interrupts from timer or external pin.		40		nA
Deep sleep current, example 3, V_{BAT} = 3 V	Ids3	As Ids2 but with 8 kB RAM data retention.		100		nA
Standby Mode current, VBAT = 3 V	Istb	Digital blocks and memories are not clocked and are powered at a reduced voltage.		17		µA
ULPMark CP 3.0 V		Arm Cortex−M3 processor running from RAM, VBAT= 3.0 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1090		ULP Mark
ULPMark CP 2.1 V		Arm Cortex−M3 processor running from RAM, VBAT= 2.1 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1260		ULP Mark
ULPMark CP 3.0 V		Arm Cortex−M3 processor running from RAM, VBAT= 3.0 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1090		ULP Mark
ULPMark CP 2.1 V		Arm Cortex−M3 processor running from RAM, VBAT= 2.1 V, IAR C/C++ Compiler for ARM 8.20.1.14183		1260		ULP Mark
Arm Cortex−M3 processor running from RAM		At 48 MHz SYSCLK. Using the IAR 8.10.1 C compiler, certified		159		Core Mark
LPDSP32 running from RAM		At 48 MHz SYSCLK Using the 2020.03 release of the Synopsys LPDSP32 C compiler		174		Core Mark
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK		123		Core Mark/ mA
Arm Cortex−M3 processor and LPDSP32 running from RAM, VBAT = 3 V		At 48 MHz SYSCLK		293		Core Mark/ mA
Arm Cortex−M3 processor running CoreMark from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK		29.1		µA/MHz

Table 5.4 ELECTRICAL PERFORMANCE SPECIFICATIONS

Description	Symbol	Conditions	Min	Typ	Max	Units
Arm Cortex−M3 processor running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK		12.3		µA/MHz
Arm Cortex−M3 processor running CoreMark from Flash, VBAT = 1.25 V		At 48 MHz SYSCLK		34.3		µA/MHz
Arm Cortex−M3 processor running CoreMark from Flash, VBAT = 3 V		At 48 MHz SYSCLK		14.6		µA/MHz
LPDSP32 running CoreMark from RAM, VBAT = 1.25 V		At 48 MHz SYSCLK		19.5		µA/MHz
LPDSP32 running CoreMark from RAM, VBAT = 3 V		At 48 MHz SYSCLK		8.2		µA/MHz
Supply voltage: operating range	VDDC		0.92	1.15	1.32 (Note 4)	V
Supply voltage: trimming range	$VDDC_{RANGE}$		0.75		1.38	V
Supply voltage: trimming step	$VDDC_{STEP}$			10		mV
Supply voltage: operating range	VDDM		1.05	1.15	1.32 (Note 5)	V
Supply voltage: trimming range	$VDDM_{RANGE}$		0.75		1.38	V
Supply voltage: trimming step	$VDDM_{STEP}$			10		mV
Supply voltage: operating range	VDDRF		1.00	1.10	1.32 (Notes 6 and 7)	V
Supply voltage: trimming range	$VDDRF_{RANGE}$		0.75		1.38	V
Supply voltage: trimming step	$VDDRF_{STEP}$			10		mV
Digital I/O supply	VDDO		1.1	1.25	3.3	V
VBAT range when the DC−DC converter is active (Note 8)	DCDC IN_RANGE		1.4		3.3	V
VBAT range when the LDO is active	LDO IN_RANGE		1.1		3.3	V
Output voltage: trimming range	DCDC OUT_RANGE		1.1	1.2	1.32	V
Supply voltage: trimming step	$DCDC_{STEP}$			10		mV
POR voltage	$VBAT_{POR}$		0.4	0.8	1.0	V
RF input impedance	Z_{in}	Single ended		50		Q
Data rate FSK / MSK / GFSK	R_{FSK}	OQPSK as MSK	62.5	1000	3000	kbps
Data rate 4−FSK					4000	kbps
On−air data rate	bps	GFSK	250		2000	kbps

5.2 RFE Specifications

Table 5.5 RF General Specifications

Description	Symbol	Conditions	Min	Typ	Max	Units
Xtal frequency	F_{XTAL}	Fundamental		48		MHz
Settling time				0.5	1.5	ms
Xtal frequency	F_{XTAL}	Fundamental		48		MHz
Settling time				0.5	1.5	ms
Frequency range	F_{RF}	Supported carrier frequencies	2360		2500	MHz
RX frequency step		RX Mode frequency synthesizer resolution			100	Hz
TX frequency step		TX Mode frequency synthesizer resolution			600	Hz
PLL Settling time, RX	t_{PLL_RX}	RX Mode		15	25	µs
PLL Settling time, TX	t_{PLL_TX}	TX mode, BLE modulation		5	10	µs
Current consumption at 1 Mbps, V_{BAT} = 1.25 V	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle		5.6		mA
Current consumption at 2 Mbps, V_{BAT} = 1.25 V	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle		6.2		mA
Current consumption at 1 Mbps, V_{BAT} = 3 V, DC−DC	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle		3.0		mA
Current consumption at 2 Mbps, V_{BAT} = 3 V, DC−DC	$IBAT_{RFRX}$	VDDRF = 1.1 V, 100% duty cycle		3.4		mA
RX Sensitivity, 0.25 Mbps		0.1% BER (Notes 9, 10)		−96		dBm
RX Sensitivity, 0.5 Mbps		0.1% BER (Notes 9, 10)		−95		dBm
RX Sensitivity, 1 Mbps, BLE		0.1% BER (Notes 9, 10) Single−ended match to 50 Q		−93		dBm
RX Sensitivity, 2 Mbps, BLE		0.1% BER (Notes 9, 10)		−91		dBm
RSSI effective range		Without AGC		60		dB
RSSI step size				2.4		dB
RX AGC range				48		dB
RX AGC step size		Programmable		6		dB
Max usable signal level		0.1% BER		−10		dBm
Tx peak power consumption at VBAT = 1.25 V (Note 11)	$IBAT_{RFTX}$	Tx power 0 dBm, VDDRF = 1.07 V, VDDPA: off, LDO mode		8.9		mA
Tx peak power consumption at VBAT = 3 V (Note 11)	$IBAT_{RFTX}$	Tx power 0 dBm, VDDRF = 1.07 V, VDDPA: off, DC−DC mode		4.6		mA
Transmit power range		BLE or 802.15.4 OQPSK	−17		0	dBm
Transmit power step size		Full band.		1		dB
		Tx power 0 dBm. Full band. Relative to the typical value.	−1.5		1.5	dB

Power in 2nd harmonic		0 dBm mode. 50 Q for “Typ” value. (Note 12)		−62		dBm
Power in 3rd harmonic		0 dBm mode. 50 Q for “Typ” value. (Note 12)		−70		dBm
Power in 4th harmonic		0 dBm mode. 50 Q for “Typ” value. (Note 12)		−82		dBm

5.3 Other Specifications

ADC

Resolution	ADC_{RES}		8	12	14	bits
Input voltage range	ADC_{RANGE}		0		2	V
INL	ADC_{INL}		−2		+2	mV
DNL	ADC_{DNL}		−1		+1	mV
Channel sampling frequency	ADC_{CH_SF}	For the 8 channels sequentially, SLOWCLK = 1 MHz	0.0195		6.25	kHz

32 kHz ON−CHIP RC OSCILLATOR

Untrimmed Frequency	$Freq_{UNTR}$		20	32	50	kHz
Trimming steps	Steps			1.5		%

3 MHz ON−CHIP RC OSCILLATOR

Untrimmed Frequency	$Freq_{UNTR}$		2	3	5	MHz
Trimming steps	Steps			1.5		%
Hi Speed mode	Fhi			10		MHz

32 kHz ON−CHIP CRYSTAL OSCILLATOR

Output Frequency	Freq32k	Depends on xtal parameters		32768		Hz
Startup time				1	3	s
Internal load trimming range		Steps of 0.4 pF	0		25.2	pF
Duty Cycle			40	50	60	%

DC CHARACTERISTICS OF THE DIGITAL PADS − With VDDO = 2.97 V – 3.3 V, nominal: 3.0 V Logic

Voltage level for high input	V_{IH}		2		VDDO+0.3	V
Voltage level for low input	V_{IL}		VSSD−0.3		0.8	V

DC CHARACTERISTICS OF THE DIGITAL PADS − With VDDO = 1.1 V – 1.32 V, nominal: 1.2 V Logic

Voltage level for high Input	V_{IH}		0.65*VDDO		VDDO+0.3	V

Voltage level for low input	V_{IL}		VSSD−0.3		0.35* VDDO	V

DIO DRIVE STRENGTH

DIO drive strength	IDIO		2	12	12	mA

FLASH SPECIFICATIONS

Endurance of the 384 kB of flash			10000			write/ erase cycles
Endurance for sections NVR1, NVR2, and NVR3 (6 kB in total)			1000			write/ erase cycles
Retention			25			years

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. The maximum VDDC voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
2. The maximum VDDM voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
3. The maximum VDDRF voltage cannot exceed the VBAT input voltage or the VCC output from the buck converter.
4. The VDDRF calibrated target is 1.07 V (TX power = 0 dBm).
5. The LDO can be used to regulate down from VBAT and generate VCC. For VBAT values higher than 1.5 V, the LDO is less efficient, and it is possible to save power by activating the DC−DC converter to generate VCC.
6. Signal generated by RF tester.
7. Single−ended match to 50 ohms, measured at pin E1 including loss of integrated Tx harmonic filter.
8. All values are based on evaluation board performance, including the harmonic filter loss.
9. The values shown here are including integrated RF filter.

Table 5.6 VDDM TARGET TRIMMING VOLTAGE IN FUNCTION OF VDDO VOLTAGE

VDDM Voltage (V)	DIO_PAD_CFG DRIVE	Maximum VDDO Voltage (V)
1.05	1	2.7
1.05	0	3.2
1.10	0	3.3

NOTE: These are trimming targets at room/ATE temperature 25 30 C.

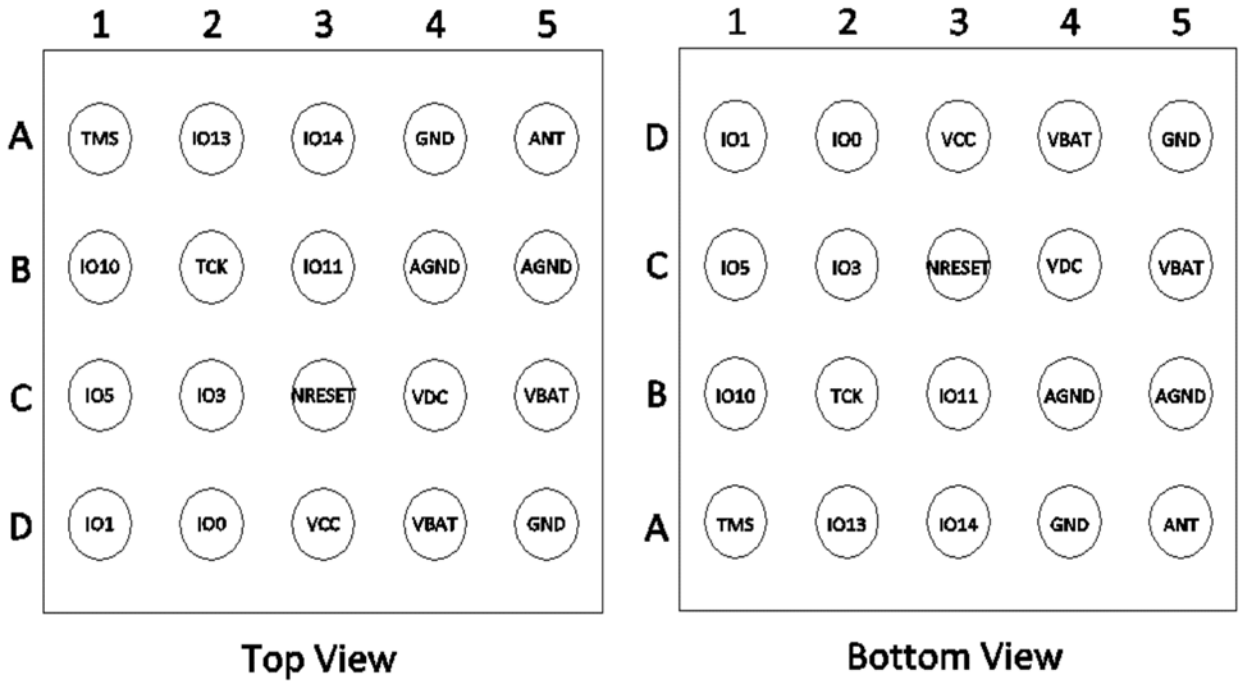
Table 5.7 VDDC TARGET TRIMMING VOLTAGE IN FUNCTION OF SYSCLK FREQUENCY

VDDC Voltage (V)	Maximum SYSCLK Frequency (MHz)	Restriction
0.92	24	The ADC will be functional in low frequency mode and between 0 and 85 C only.
1.00	24	Fully functional
1.05	48	Fully functional

NOTE: These are trimming targets at room/ATE temperature 25 30 C.

6. Pin layout view and Pin Description

6.1 Pin layout view



6.2 Pin Description

Pin#	Pin Def	Pin Name	Pin Function	Pin Description
1	A1	TMS	I/O	Test Mode Select
2	A2	IO13	I/O	I/O
3	A3	IO14	I/O	I/O
4	A4	GND	GND	GND
5	A5	ANT	RF	RF signal input/output (Antenna)
6	B1	IO10	I/O	I/O
7	B2	TCK	I/O	External clock input
8	B3	IO11	I/O	I/O
9	B4	AGND	AGND	AGND
10	B5	AGND	AGND	AGND
11	C1	IO5	I/O	I/O
12	C2	IO3	I/O	I/O
13	C3	NRESET	I/O	Reset
14	C4	VDC	VDC	DC−DC output voltage to external LC filter
15	C5	VBAT	Power Source	Power Source
16	D1	IO1	I/O	I/O
17	D2	IO0	I/O	I/O
18	D3	VCC	VCC	DC−DC filtered output
19	D4	VBAT	VBAT	VBAT
20	D5	GND	GND	GND

7.PCB Guidelines and SMT Guidelines

7.1 PCB Design Guidelines

1. Decoupling capacitors should be placed as close to the related balls as possible.
2. Differential output signals should be routed as symmetrically as possible.
3. Analog input signals should be shielded as well as possible.
4. Pay close attention to the parasitic coupling capacitors.
5. Special care should be made for PCB design in order to obtain good RF performance.
6. Multi−layer PCB should be used with a keep−out area on the inner layers directly below the antenna matching circuit in order to reduce the stray capacitances that influence RF performance.
7. All the supply voltages should be decoupled as close as possible to their respective pin with high performance RF capacitors. These supplies should be routed separately from each other and if possible on different layers with short lines on the PCB from the chip's pin to the supply source.
8. Digital signals shouldn't be routed close to the crystal or the power supply lines.
9. Proper DC−DC component placement and layout is critical to RX sensitivity performance in DC−DC mode.

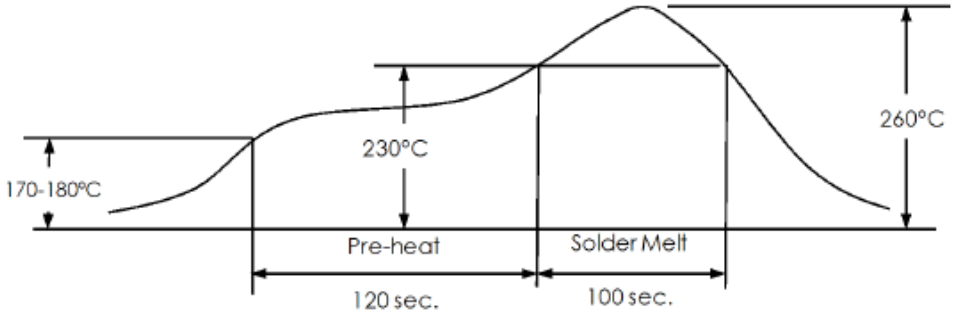
7.2 SMT Solder Information

The RSL10 SIP is constructed with all RoHS compliant material and should be reflowed accordingly. This device is Moisture

Sensitive Class MSL3 and must be stored and handled accordingly. Re−flow according to IPC/JEDEC standard J−STD−020C,

Joint Industry Standard: Re−flow Sensitivity Classification for Nonhermetic Solid State Surface Mount Devices. Hand soldering is not recommended for this part.

For more information, see SOLDERRM/D available from www.onsemi.com.

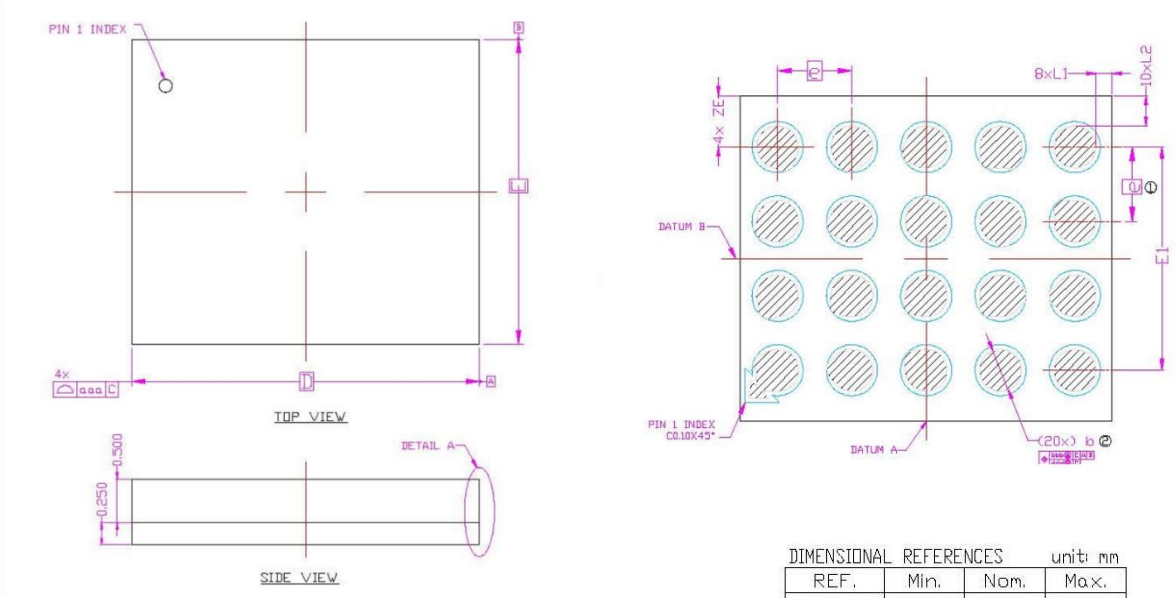


Stage	Temperature Profile	Time (maximum)
Pre-heat	170 ~ 180°C	120 sec.
Solder Melt	Above 230°C	100 sec.
Peak	260°C maximum	30 sec.

Figure 7.1 SOLDER FLOW PROFILE

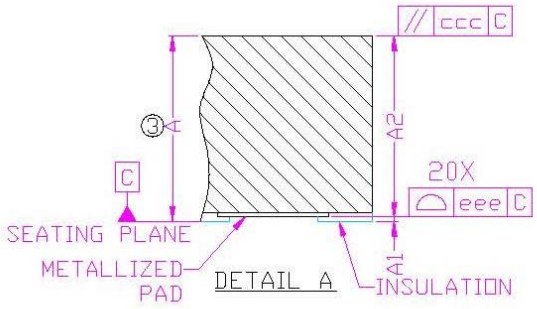
8.Package Outline

REV	DESCRIPTION	DATE	DESIGNER	REVIEWER	APPROVER
A	Initial Release	2022-MAR-04	NancyJiang	DENNIS	JI HAIJIAN



DIMENSIONAL REFERENCES unit: mm

REF.	Min.	Nom.	Max.
A	0.69	0.75	0.81
A1	–	–	0.03
A2	–	–	0.78
b	0.40	0.45	0.50
D	3.95	4.00	4.05
E	3.45	3.50	3.55
E1	2.40 BSC		
ZE	0.55 BSC		
e	0.80 BSC		
L1	0.125	0.175	0.225
L2	0.275	0.325	0.375



DIMENSIONAL REFERENCES unit: mm

REF.	TOLERANCE OF FORM AND POSITION
aaa	0.10
bbb	0.10
ccc	0.10
ddd	0.08
eee	0.08

Notes :

① 'e' REPRESENTS THE BASIC TERMINAL PITCH. SPECIFIES THE TRUE GEOMETRIC POSITION OF THE TERMINAL AXIS.

② DIMENSION 'b' APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.00mm AND 0.25mm FROM TERMINAL TIP.

③ DIMENSION 'A' INCLUDES PACKAGE WARPAGE.

④ EXPOSED METALLIZED PADS ARE CU PADS WITH SURFACE FINISH PROTECTION.

⑤ PACKAGE DIMENSIONS TAKE REFERENCE TO JEDEC MO-208 REV.C.

9.Ordering Information

Contact: sales@jhearing.com

PUBLICATION ORDERING INFORMATION

TECHNICAL SUPPORT tech@jhearing.com **Email Requests to** sales@jhearing.com **Website** www.jhearing.com